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POWER AND PERFORMANCE EFFICIENT TOPOLOGICALLY COMPRESSED DUAL VDD FLIP FLOP

Venkata K. Ramanaiah
Dept. of ECE, YSR Engineering college of Yogi Vemana University, Proddatur, Andhra Pradesh, India

ABSTRACT

The very low power and high speed dual VDD Flip Flop (FF) is proposed in this paper. The power reduction has achieved by introducing dual VDD technique with two different supply voltages as Vdd1 and Vdd2. The small number of MOS transistors are connected to clock signal, reduces drastic leakage power consumption, and the smaller no of transistor count makes the cell area equals to conventional FFs. In addition, fully static full-swing operation makes the cell tolerant of supply voltage and input slew variation. With dual VDD, topologically compressed flip flop gives 82.72% improvement over power, delay and power delay product and the nontopologically compressed flip flop gives only 30.79% improvement as compared with conventional flip flops. An experimental chip design is carried out by 90 nm CMOS technology.

KEYWORDS: Dual VDd, Flip Flop, power, delay,Efficent topology.

INTRODUCTION

Flip-Flop is an electronic circuit that stores a sensible state of one or more information data motions because of a clock pulse. Flip-flops are regularly utilized as a part of Computational circuits to work in chose successions within repeating clock interims to get and keep up information for a constrained time period .At each one ascending or falling edge of a clock pointer, the information put away in a set of flip-flops is promptly accessible so it might be connected as inputs to other combinational or consecutive Circuitry. Delay Flip-Flop (DFF) has been the necessary piece of any digital structure to build the sequential piece of it. To accomplish low power, low space we have plan different D flip-flop to examine the execution of different architectures of DFF regarding execution measurements, for example, power, delay, space and Power Delay Product (PDP).

However as innovations scales down to the nanometre administration (Deep Sub- Micron (DSM)), the static power utilization gets to be more significant than the dynamic power utilization [3].
With technology downscaling, interconnect resistance and capacitance build the propagation interval. Leakage power improvement will be a key outline objective in future CMOS circuits. Power will keep on being a constraining variable in future advances [3].

Design factors desirable for flip flop

- High speed
- Low power consumption
- Robustness and noise stability
- Small area and less number of transistor

EXISTING METHOD

DIFFERENTIAL SENSE-AMPLIFIER FLIP-FLOP:

Fig 1 shows a typical circuit of differential sense-amplifier type FF [1]-[3]. This type of circuit is very effective to amplify small-swing signals, so is generally used in output of memory circuits. In this FF, however, the effect of power reduction goes down in the condition of lower data activity, because these kinds of circuits have pre-charge operation in every clock-low state. Moreover, if we use reduced clock swing, a customized clock generator and an extra bias circuit are necessary.

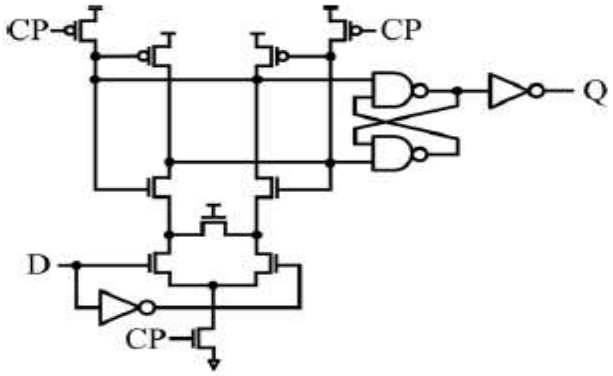

Fig 1: Differential Sense-Amplifier Flip Flop

CONDITIONAL-CLOCKING FLIP-FLOP :

Figure 2 shows the conditional clocking type FF (CCFF) [4]-[6]. This circuit is achieved from a functional point of view. The circuit monitors input data change in every clock cycle and disables the operation of internal clock if input data are not changed. By this operation, power is reduced when input data are not changed. But unfortunately, its cell area becomes almost double that of the conventional circuit shown in Fig. 3.1. And mainly due to this size issue, it becomes hard to use if the logic area is relatively large in the chip.

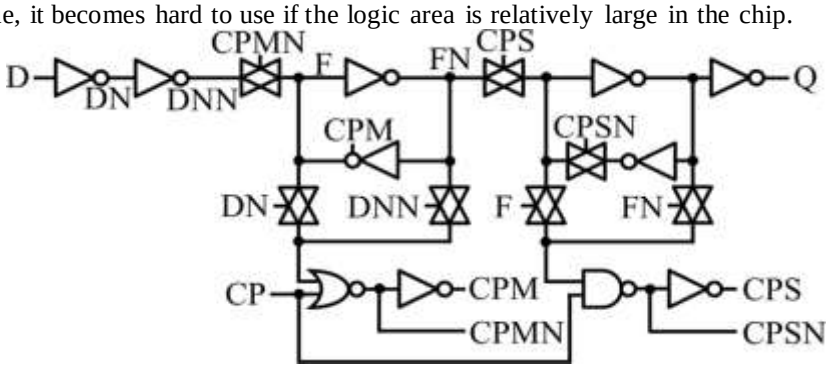

Fig 2: Conditional-clocking Flip Flop (CCFF)

CROSS-CHARGE CONTROL FLIP- FLOP:

Fig 3 shows the circuit of cross-charge control FF (XCFF) [7]. The feature of this circuit is to drive output transistors separately in order to reduce charged and discharged gate capacitance. However, in actual operation, some of the internal nodes are pre-set with clock signal in the case of data is high, and this operation dissipates extra power to charge and discharge internal nodes. As a result, the effect of power reduction will decrease. Circuits including pre-set operation have the same problem.

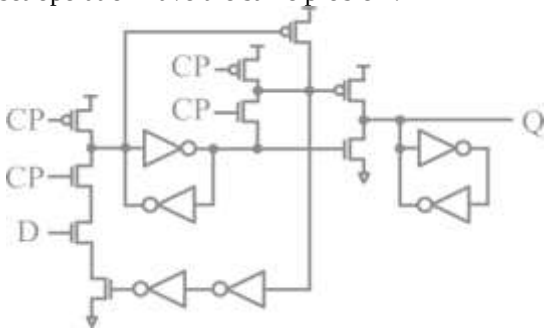

Fig 3: Cross-charge control flip- flop (XCFF)

ADAPTIVE-COUPLING FLIP-FLOP:

The adaptive-coupling type FF (ACFF) [9] shown in Figure 4 is based on a 6-transistor memory cell. In this circuit a single- channel transmission-gate with additional dynamic circuit has been used for the data line in order to reduce clock-related transistor count. However, in this circuit, delay is easily affected by input clock slew variation because different types of single- channel transmission-gates are used in the same data line and connected to the same clock signal. Moreover, characteristics of single-channel transmission-gate circuits and dynamic circuits are strongly affected by process variation. Thus, their optimization is relatively difficult, and performance degradation across various process corners is a concern.

Let us summarize the analysis on previously reported low- power FFs. For Diff FF [1] and XCFF [7], pre-charge operation is a concern especially in lower data activity. As regards CFF, its cell area becomes a bottleneck to use. And for ACFF, tolerance for input clock slew variation becomes subject to resolve.

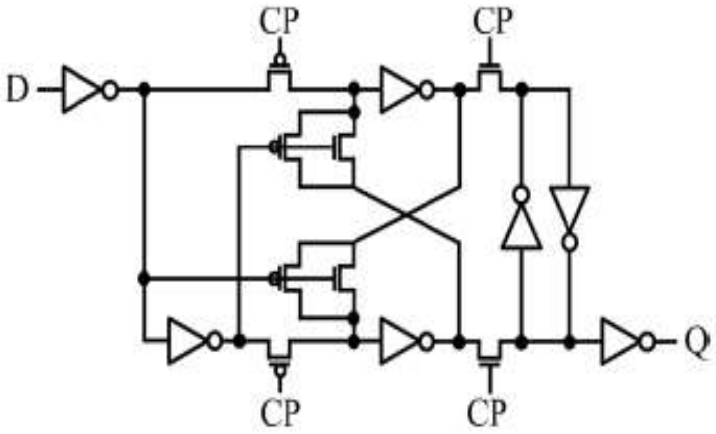

Fig 4: Adaptive-coupling flip-flop

COMBINATIONAL TYPE FLIP- FLOP:

In order to reduce the power of the FF while keeping competitive performance and similar cell area. To reduce the transistor count, especially those operating with clock signals, without introducing any dynamic or pre-charge circuit. The power of the FF is mostly dissipated in the operation of clock-related transistors, and reduction of transistor count is effective to avoid cell area increase and to reduce load capacitance in internal nodes.

In the conventional FF there are 12 clock-related transistors. To reduce clock-related transistor counts directly from this circuit is quite difficult. One reason is because transmission-gates need a 2-phase clock signal, thus the clock driver cannot be eliminated. Another reason is that transmission-gates should be constructed by both PMOS and NMOS to avoid degradation of data transfer characteristics caused by single-channel MOS usage. Therefore, instead of transmission-gate type circuit, combinational type circuit is as shown in Fig 5.

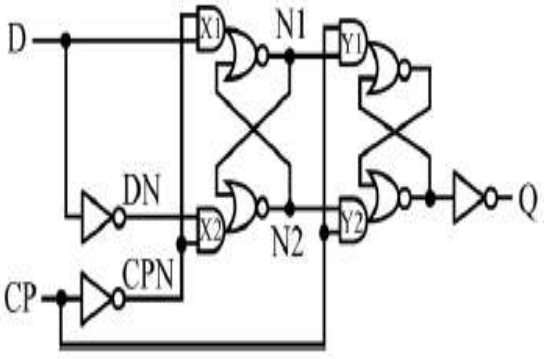

Fig 5 Combinational Type Flip Flop

To reduce the transistor-count based on logical equivalence, considering a method consisting of the following two steps. As the first step, we plan to have a circuit with two or more logically equivalent AND or OR logic parts which have the same input signal combination, especially including clock signal as the input signals. Then, merge those parts in transistor level as the second step.

PROPOSED METHOD

Employing dual supply voltages is attractive for reducing the power consumption without sacrificing the speed of the circuit. The increased power dissipation degrades the reliability, increases the cost of the packaging and cooling system, and lowers the battery lifetime in portable electronic devices. An effective method for reducing the power consumption is scaling the supply voltage. Dynamic, short-circuit, and leakage components of power consumption are simultaneously reduced with the scaling of the supply voltage in a CMOS circuit.

Lowering the supply voltage, however, also degrades the circuit speed. The dual VDD circuit technique exploits the delay differences among the different signal propagation paths within an IC. The supply voltages of the gates on the non-critical delay paths are selectively lowered while a higher supply voltage is maintained on the critical delay paths in order to satisfy a target clock frequency in a multi-VDD circuit. Similarly, in systems-on chips (SoCs), different circuits operating at different supply voltages exist.

Design for low power has become a key requirement in today's SoC design, especially for mobile applications. Dual V_{dd} is an effective method to reduce both leakage and dynamic power, by assigning different supply voltages to cells according to their timing criticality. In a multi-V_{dd} design, cells of different supply voltage are often grouped into small number of voltage islands (each having a single supply voltage), in order to avoid complex power supply system and excessive amount of level shifters (as the former would cause increase in design cost and the latter would cause extra overhead in area, delay and power). In proposed method, a low power design methodology which manages power, timing and design cost by using dual V_{dd}

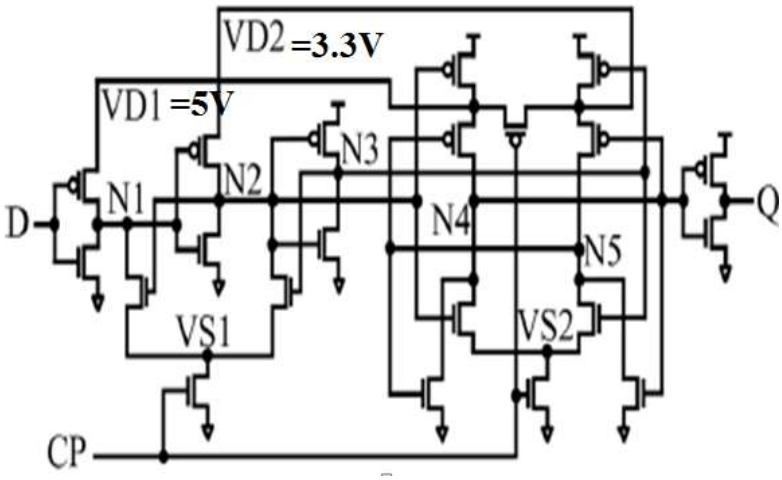

Fig 6: Topologically compressed dual VDD FlipFlop

Fig 6 shows the topologically compressed flip flop with dual V_{dd} technique with two different supply voltages as VDD1=5v and VDD2 = 3.3v. The existing method is working with only 5v supply voltage where as the proposed method is working with dual V_{dd} technique with two different supply voltages. For TTL 5V is necessary and CMOS can operate at various voltage levels like 5V, 3.3V, 2.5V, 1.2V, 1V etc. As SSI and MSI devices require interfacing between these two for developing low power and high speed circuits at MSI to VLSI level. So in proposed method two supply voltages are using as 5V and 3.3V in the project.

In proposed method the delay, power and power delay product is reduced. With dual V_{dd} technique, TCFF gives 87.72% improvement over conventional flip flop and without dual V_{dd}, TCFF is 30.79% better than the conventional flip flop. Hence TCFF with multi V_{dd} is better suited to desired applications.

When CP is low, the PMOS transistor connected to CP turns on and the master latch becomes the data input mode, and the input data from D is stored in the master latch. When CP is high, the PMOS transistor connected to CP turns off, the NMOS transistor connected to CP turns on, and the slave latch becomes the data output mode. In this condition, the data in the master latch is transferred to the slave latch, and then outputted to Q. In this operation, all nodes are fully static and full-swing. The current from the power supply does not flow into the master and the slave latch simultaneously because the master latch and the slave latch become active alternately. Therefore, timing degradation is small on cell performance even though many transistors are shared with no increase in transistor size.

RESULTS AND DISCUSSION

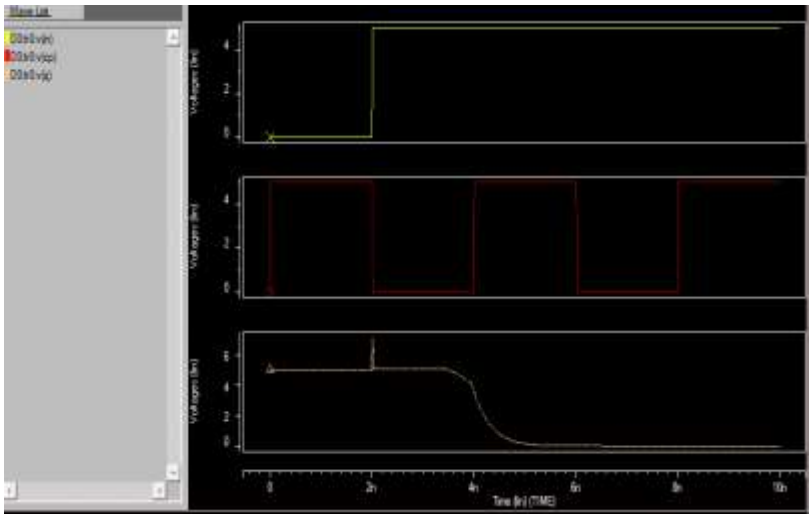

Fig 7: Output Waveform for Topologically Compressed Flip Flop with Dual V_{dd}

Fig. 7: shows the spice simulation waveforms for topologically compressed dual VDD flip flop with dual power supply as 5v and 3.3v. The overall reduction in power, delay and power delay product is about 82.72 % when compared with conventional flip flop.

Table 1. Comparison table FFs

Existing Methods/Proposed	Type of Flip Flop	Average Power (W)	Delay (pSec)	PDP (pJoules)
conventional	Transistor level schematic of flip flop	1.6320	8.3047	13.5532
Nontopological	Transistor level schematic of topologically compressed flip flop (TCFF)	0.61828	5.1823	3.2041
Proposed	TC Dual VDD FF	0.17884	1.9997	0.3575

CONCLUSION

An extremely low-power flip flop called topologically compressed flip flop is proposed with dual V_{dd} technique. In this project dual V_{dd} technique is applied which reduces the power delay and power delay product by 82.72% as compared to conventional flip flops. In addition, fully static full-swing operation makes the cell tolerant of supply voltage and input slew variation. An experimental chip design is carried out by 90 nm CMOS technology.

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AUTHOR BIBLIOGRAPHY

Venkata K.Ramanaiah received the M.Tech. and Ph.D. degrees in electronics and communications engineering from J.N.T.University, Hyderabad, in 1999 and 2009, respectively. He is currently working as associate professor in the dept. of ECE at YSR Engineering college of Yogi Vemana University, Produttut, India. His current research interest includes in the areas VLSI, Image processing, and Neural Networks. He is the author and co-author for around 45 publications.